What is claimed is:

1. A semiconductor memory device comprising:

a cell array having a plurality of memory cells;

a plurality of first normal elements each defined within said cell array as a group of memory cells arranged in a first direction with a first select line for memory cell selection;

a plurality of second normal elements each defined within said cell array as a group of memory cells arranged in a second direction with a second select line for memory cell selection, each said second normal element selecting one or more memory cells in operative association with a corresponding one of said first normal elements;

a plurality of first redundant elements disposed for replacement of a defective first normal element within said cell array;

a plurality of second redundant elements disposed for replacement of a defective second normal element within said cell array;

first repair regions each defined within said cell array as a group of first normal elements with permission of replacement by each said first redundant element; and

second repair regions each defined within said cell array as a group of second normal elements with permission of replacement by each said second redundant element, wherein

at least two of said plurality of first normal

elements are activated simultaneously,

whether each of such simultaneously activated at least two first normal elements is replaced by said first redundant element is controlled independently of each other, and

at least one of said second redundant elements, which repairs a second normal element having a defect that locates in one of said first repair regions including one of said simultaneously activated at least two first normal elements, does not intersect said one of said simultaneously activated at least two first normal elements.

2. The semiconductor memory device according to claim 1, wherein said second normal element having a defect that locates in one of said first repair regions including one of said simultaneously activated at least two first normal elements is also replaceable by one of said plurality of second redundant elements which intersect said one of said simultaneously activated at least two first normal elements.

3. The semiconductor memory device according to claim 1, wherein one of said first repair regions including one of said simultaneously activated at least two first normal elements and another one of said first repair regions including another one of said simultaneously activated at least two first normal elements are disposed adjacent to each other, one of said

second redundant elements intersecting said another one of said simultaneously activated at least two first normal elements and repairing a second normal element having a defect that locates in said first repair region including said one of said simultaneously activated at least two first normal elements.

4. The semiconductor memory device according to claim 1, wherein at least three first repair regions, each of which includes one of at least three simultaneously activated first normal elements, are serially disposed, and wherein

at least two said second redundant elements, which are able to repair a second normal element having a defect that locates in one of said first repair regions including one of said simultaneously activated at least three first normal elements, intersect the remaining any one of said simultaneously activated at least three first normal elements.

5. The semiconductor memory device according to claim 3, wherein a select circuit is disposed between said first repair regions disposed adjacent to each other for selecting a first normal element.

6. The semiconductor memory device according to claim 4, wherein select circuits are disposed between said first repair regions disposed serially for selecting a first normal element.

7. The semiconductor memory device according to

claim 1, wherein

said cell array comprises first and second memory arrays neighboring each other with a row decoder interposed therebetween;

said first normal elements in said first and second memory arrays are simultaneously activated by said row decoder in a row address responsive manner in such a way that at least one is selected from each of said first and second memory array;

said plurality of first redundant elements are disposed in correspondence with said first and second memory arrays in such a manner as to belong thereto on at least one-by-one basis, and used independently of each other for defective first normal element replacement within said first and second memory arrays, respectively; and

said plurality of second redundant elements are disposed in correspondence with said first and second memory arrays in such a manner as to belong thereto on at least one-by-one basis while intersecting said first redundant elements in correspondence with each of said first and second memory array, and used independently of each other for defective second normal element replacement within both of said first and second memory arrays.

8. The semiconductor memory device according to claim 7, further comprising:

column decoders for selecting second normal elements

of said first and second memory arrays, respectively;

redundant row decoders activated by row replacement control signals as generated in response to defective row addresses for activating said first redundant elements, respectively;

redundant column decoders activated by column replacement control signals as generated in response to defective column addresses for selecting said second redundant elements, respectively; and

a replacement control circuit configured to output said row replacement control signals and column replacement control signals in accordance with defect addresses, and to have such an overlap region that one of said first repair regions defined within one of said first and second memory arrays and one of said second repair regions are at least partially overlapped, said one of said first repair regions being defined as that said first normal elements therein are replaceable by said first redundant element disposed in correspondence with said one of said first and second memory arrays, said one of said second repair regions being defined as that said second normal elements therein are replaceable by said second redundant element disposed in the remaining one of said first and second memory arrays.

9. The semiconductor memory device according to claim 7, wherein each of said first repair regions to which said first redundant elements are assigned is

defined in either of said first and second memory arrays, respectively, and wherein at least one of said second repair regions to which said second redundant elements are assigned is defined as extending over said first and second memory arrays.

10. The semiconductor memory device according to claim 4, wherein

said cell array comprises three or more memory arrays serially disposed with row decoders interposed between adjacent ones thereof for simultaneous selection of first normal elements in a row address responsive manner in a way such that at least one is selected from each memory array,

said plurality of first redundant elements are disposed in correspondence to the respective memory arrays in such a manner as to belong thereto on at least one-by-one basis to replace a defective first normal element therein independently of each other, and

said plurality of second redundant elements are disposed within the respective memory arrays in such a manner as to belong thereto on at least one-by-one basis while crossing said first redundant element within a corresponding memory array, and are used independently of each other for defective second normal element replacement within at least one presently selected memory array.

11. The semiconductor memory device according to claim 1, wherein

each of said first normal element comprises one or a plurality of word lines as said first select line,

each of said first redundant element comprises one or a plurality of spare word lines,

each of said second normal element comprises one or a plurality of bit lines selected by a single column address, and

each of said second redundant element is one or a plurality of spare bit lines selected by a single defective column address.

12. The semiconductor memory device according to claim 7, wherein said first repair regions are row repair regions as defined by said row redundant elements, each row repair region covering an entirety of each said memory array, and

wherein when letting an all-cell capacity of each memory array be represented by C [bits], said second repair region comprises a first column repair region with a capacity of 2C/M (M is an integer greater than or equal to 3) as set including N (N is an integer greater than or equal to 2) redundant column elements in each memory array, (M-1)/2 first column repair regions being defined in each said memory array, and a second column repair region with a capacity of 2C/M as set including N redundant column elements while combining together two remaining capacity C/M regions of respective ones of said memory arrays.

13. The semiconductor memory device according to

claim 12, wherein said first column repair region is a normal data area, whereas said second column repair region is a parity data area for storing therein check-use data for error checking/correcting data of said normal data area.

14. The semiconductor memory device according to claim 7, wherein each said memory array is subdivided into a plurality of sub-arrays with the same row address allocated thereto for simultaneously activating a specified number of ones at a time, and

a single spare column select line as continuously formed to span said plurality of sub-arrays is allocated to different row addresses to be used as said plurality of redundant column elements.

15. The semiconductor memory device according to claim 1, wherein said cell array has a plurality of memory arrays, a plurality of main word lines provided to span these memory arrays, a plurality of sub-word lines disposed within each said memory array at least one of which is selected by the corresponding main word line in each said memory array, at least one spare main word line provided to span said plurality of memory arrays, and at least one spare sub-word line disposed in each said memory array at least one of which is selected by the corresponding spare main word line in each said memory array, and

said sub-word lines are for use as said first normal

elements, whereas said spare sub-word line in each said memory array is used as said first redundant element.

16. A semiconductor memory device comprising:

simultaneously activated first and second memory arrays each having a plurality of memory cells, a plurality of normal row elements each defined in said memory arrays as a group of memory cells arranged in a row direction, and a plurality of normal column elements each defined in said memory arrays as a group of memory cells arranged in a column direction;

redundant row elements disposed in correspondence to said first and second memory arrays to be used for defective normal row element replacement in the respective memory arrays independently of each other; and

redundant column elements disposed in correspondence to said first and second memory arrays in such a manner that at least one of them corresponds to each said memory array while intersecting said redundant row element within a corresponding memory array and used for defective normal column element replacement independently of each other, wherein

a row repair region defined as a group of normal row elements with permission for replacement by each said redundant row element disposed in one of said first and second memory arrays and a column repair region defined as a group of normal column elements with permission of replacement by use of each said redundant column element

disposed in the remaining one of said memory arrays are set to have an overlap region in which said row and column repair regions are at least partially overlapped each other.

17. The semiconductor memory device according to claim 16, wherein said redundant column element within a memory array to which said overlap region belongs is also used for replacement of a defective normal column element in such overlap region.

18. The semiconductor memory device according to claim 16, wherein said first and second memory arrays are disposed adjacent to each other with a row decoder commonly shared thereby interposed therebetween, and wherein said row decoder is arranged for simultaneously selecting two normal row elements each belonging to said first and second memory arrays.

19. The semiconductor memory device according to claim 16, wherein said normal row element comprises one or a plurality of word lines, said redundant row element comprises one or a plurality of spare word lines, said normal column element comprises one or a plurality of bit lines selected by a single column address, and said redundant column element comprises one or a plurality of spare bit lines selected by a single defective column address.

20. The semiconductor memory device according to claim 16, wherein said first repair regions are row repair

regions each covering an entirety of each said memory array as defined by row redundant elements disposed in correspondence with said memory arrays respectively on at least one-by-one basis, and

wherein when letting an all-cell capacity of each memory array be represented by C [bits], said second repair region comprises a first column repair region with a capacity of 2C/M (M is an integer greater than or equal to 3) as set including N (N is an integer greater than or equal to 2) redundant column elements in each memory array, (M-1)/2 first column repair regions being defined in each said memory array, and a second column repair region with a capacity of 2C/M as set including N redundant column elements while combining together two remaining capacity C/M regions of respective ones of said memory arrays.

21. The semiconductor memory device according to claim 16, wherein said first column repair region is a normal data area, whereas said second column repair region is a parity data area for storing therein check data for error checking/correcting data of said normal data area.

22. The semiconductor memory device according to claim 16, wherein each said memory array is divided into a plurality of sub-arrays with the same row address being allocated thereto for simultaneously activating a specified number of sub-arrays at a time, and

a single spare column select line as continuously formed to span said plurality of sub-arrays is allocated

to different row addresses to be used as said plurality of redundant column elements.

23. A semiconductor memory device comprising:

a cell array having a plurality of memory cells;

a plurality of main word lines disposed in said cell array;

a plurality of sub-word lines simultaneously selectable upon activation of each said main word line, each said sub-word line being for selecting more than one memory cell disposed within a specified range in a row direction;

a plurality of column select lines for execution of memory cell selection in association with each of said sub-word line;

at least one spare main word line disposed for repairing a defective cell; and

a plurality of spare sub-word lines simultaneously selected by said spare main word lines, each of said spare sub-word line being for performing spare cell selection within a specified range in the row direction, wherein

when any one of said plurality of sub-word lines selected by a certain main word line is found defective, the defective sub-word line is made inactive while letting a presently selected main word line stay active, whereas said spare main word line is activated, thereby permitting activation of one of a plurality of spare sub-word lines, as selected by this spare main word line, which is used

for replacement of the defective sub-word line.

24. The semiconductor memory device according to claim 23, further comprising more than one spare column select line for repairing said column select lines, wherein a defective column select line for performing memory cell selection in association with a certain sub-word line is replaced by the spare column select line for spare cell selection in association with another sub-word line to be activated simultaneously along with the sub-word line.

25. The semiconductor memory device according to claim 24, further comprising another spare column select line for replacement of said column select line, wherein a defective column select line for performing memory cell selection in association with a certain sub-word line is also replaced by said another spare column select line for spare cell selection in association with the sub-word line.

26. A semiconductor memory device comprising:

a cell array having a plurality of memory cells, a plurality of normal row elements each defined in said cell array as a group of memory cells arranged in a row direction, and a plurality of normal column elements each defined in said cell array as a group of memory cells arranged in a column direction;

a plurality of redundant row elements disposed for repairing more than one defective normal row element of said cell array; and

a plurality of redundant column elements disposed for repairing more than one defective normal column element of said cell array, wherein

at least two first and second row repair regions, each of which is defined as a group of normal row elements with permission of replacement by each said redundant row element, are set to have different cell capacities with each other, and

repair efficiency in each column repair region defined as a group of normal column elements with permission of replacement by each of said plurality of redundant column elements is set to become equal to one another within said cell array.